Pixel Opto-link Specifications

K. Einsweiler, LBNL

Critical for evaluation of DORIC/VDC designs to have specs

- Global light budget for TTC links and Data links is first step
- Several open issues to resolve in basic features of electronics, including VDC/ DORIC polarity, and number of independent supplies and their multiplicity.

Show first draft of global light budget today:

- Start from SCT template, discuss with many experts (Tony W, Peter D, Ming-Lee C)
- Further discussion and iteration needed.

Ingredients for light budget:

TTC Link:

- Coupled optical power from BOC OptoTx Module VCSEL into Fiber, including loss in opto-module MT connector.
- Light loss in fiber, in connectors (expected at PP4, PP2, and PP1), and in GRIN/SIMM transition (expected at PP2).
- Transformation of optical power into Taiwan 8:1 opto-package PIN current.
- Additional losses in fiber transmission or PIN responsivity due to irradiation.

Data Link:

- Coupled optical power from Taiwan 8:1 opto-package VCSEL into Fiber, including loss in splicing (if present).
- Light loss in fiber, in connectors (expected at PP1, PP2, and PP4), and in SIMM/GRIN transition (expected at PP2).
- Transformation of optical power into BOC OptoRX Module PIN current.
- Additional losses in fiber transmission or VCSEL light output due to irradiation.

Estimate at “nominal”, worst case, and best case values

- Some quantities will be controlled by Q/A procedures, and only parts within some spec will be selected. Other parts will be used “as is”.

TTC Link

Coupled power into fiber:

- The BOC opto-modules will have their light output measured, channel by channel, and a minimum requirement will be applied to all channels.
- First prototypes suggest Trulight arrays will produce 1mW coupled power (bias may be greater than 10mA). Lifetime is less important for off-detector transmitters.

Losses in transmission:

- No numbers for fiber losses, but expected to be “small”. Less than 1db ?
- For connector losses, claim that 1db per MT connector is worst case. Add 1db extra loss for the GRIN/SIMM transition to get a total of 4db loss (transmit 0.4 of input).
- These losses need to be checked during Q/A to prevent bad links.

Converted PIN current:

- The conversion from input optical power to PIN current will be monitored in the Taiwan package. Taiwan expect to be able to make a cut at 0.4mA/mW. SCT has used a minimum of 0.3mA/mW in their specification.

Additional losses due to irradiation:

- With larger PIN bias of up to 10V, claim no significant loss in signal is observed.
- Worst case is 120μA output. Extra 1db in fiber and PIN would give 70μA.

Data Link

Coupled power into fiber:

- The Taiwan 8:1 packages will have their light output measured, channel by channel, and a minimum requirement will be applied to all channels.
- Taiwan will use good quality Trulight VCSELs which produce 1mW optical power for 10mA bias. Estimate worst case coupling gives 0.6mW coupled optical power.

Losses in transmission:

- No numbers for fiber losses, but expected to be “small”. Less than 1db ?
- For connector losses, claim that 1db per MT connector is worst case. Add 1db extra loss for the SIMM/GRIN transition to get a total of 4db loss (transmit 0.4 of input).
- These losses need to be checked during Q/A to prevent bad links.

Converted PIN current:

- The conversion from input optical power to PIN current will be monitored in the Taiwan package. Taiwan expect to be able to make a cut at 0.4mA/mW.

Additional losses due to irradiation:

- Losses in VCSEL light output claimed to be up to 3db for operation at 10mA. Annealing with 20mA for one week reduces loss to 1db. Assume 3db worst case.
- Worst case is 48μA output. Extra 1db in fiber would give 40μA.

Temperature issues

- Qualification of parts during production will be done at room temperature.
- Opto-boards in pixels will operate at a temperature in the range of -25C to 0C.

TTC Link issues:

- The performance of the PIN diode is independent of temperature, so there should be no particular issues here.

Data Link issues:

- The main effect of the reduced temperature should be to reduce the VCSEL threshold. This will increase the light output for both the “low” and the “high” output state.
- The extra light in the “high” state should not have any negative effects.
- The VCSEL threshold should always remain well above the worst-case “low” VDC current of 1.5mA, but this needs to be checked more carefully.
- In any case, the DRX threshold is adjustable on the BOC, so modest compensation can be made for a link with too much light in the “0” state.
- General message: need a bit more data at actual operating temperature range to understand effects on VCSEL. During production testing, will want to check worst case coupled power for VCSEL-on and best case coupled power for VCSEL-off.

Comments:

Electronics specs:

- Minimum signal for DRX is specified to be 20μA (and this will be controlled during wafer probing), with claim that the chip works down to lower input levels, so there is extra margin. Awaiting data from SCT on how large the margin is.
- Note that taking advantage of low threshold in DRX may be difficult, because it may require frequent adjustment on BOC, and regular BER measurements, to keep each link “tuned” for good performance.
- In our analysis, 20μA gives 4db of safety margin (factor 2.5), which is minimal. Would prefer to increase light output from on-detector package to 1mW coupled power worst case, giving 6db margin, plus whatever safety factor is in DRX minimum threshold. Requires operating above 10mA, so some lifetime impact ?
- Minimum signal for DORIC specified to be 60μA (this must be controlled during wafer probing). Claim that it should work down to 20μA, so there is extra margin.
- In our analysis, 60μA gives about 3db margin, and 20μA gives about 8db. Suggest the DORIC spec should be changed to 20μA minimum signal, and we should work hard to meet this spec.
- Dynamic range issues (largest input signals for DRX and DORIC) need further investigation. Presently no plans to implement Q/A selection on maximum coupled power for transmitters.

Q/A issues:

- Should do whatever we can to increase the light output from the drivers, by choosing the best available VCSELs (receivers are essentially fixed). Difficult to reach 1mW coupled power at 10mA for on-detector links. We will need to verify that all transmitters and receivers meet specifications.
- In addition, we should control the fiber and fiber termination carefully to try to reduce the 4db worst case losses there. New information from Taiwan suggests using grease in MT connector could reduce worst case loss to 0.5db/connection.
- Will need to check VCSEL forward voltage for on-detector devices. Our spec (see below) requires less than 2.3V forward voltage at 20mA after irradiation. This translates to about 2.1-2.2V at the time of assembly (to be checked in more detail).

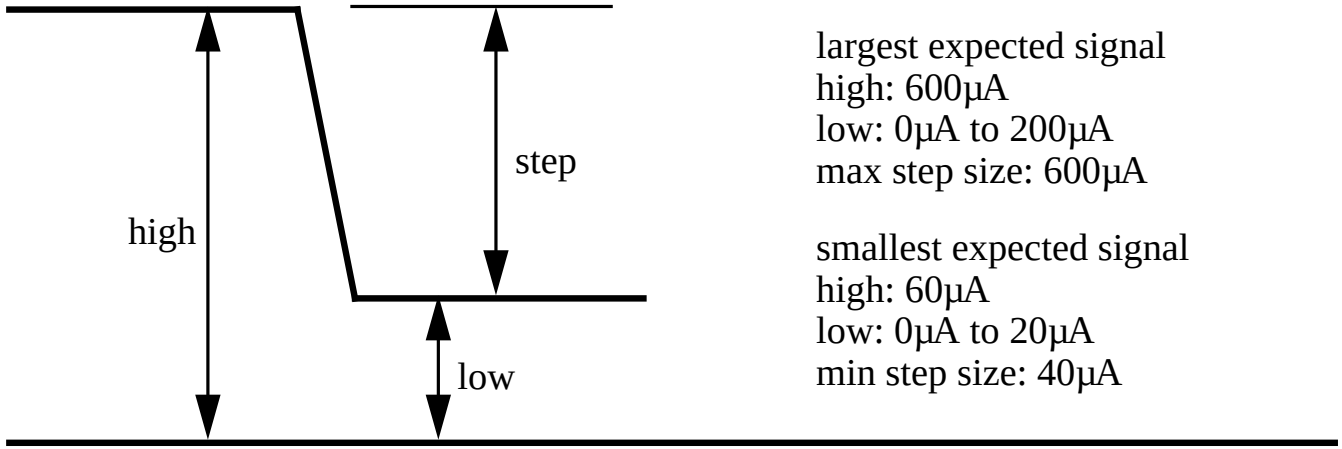
On-detector electronics power supply issue:

- Propose to operate the DORIC and VDC at 2.5V, which leaves very modest margin in lifetime (maximum process operating voltage is 2.7V for nominal IBM 10 year lifetime). Recall that in the present services scheme, this voltage is supplied directly from USA15 with no regulator at PP2, and it should have a roundtrip services voltage drop in the range of 500mV to 1V.
- The VDC will then be specified to have less than 200mV voltage drop at 20mA for its internal current source (this will have to be checked by wafer probing), so it will be capable of providing 2.3V to the VCSEL. This specification is approximately met by the current VDC design.

Summary of key opto-electronics specifications

DORIC:

- **Input signal requirements:** example from SCT specification:

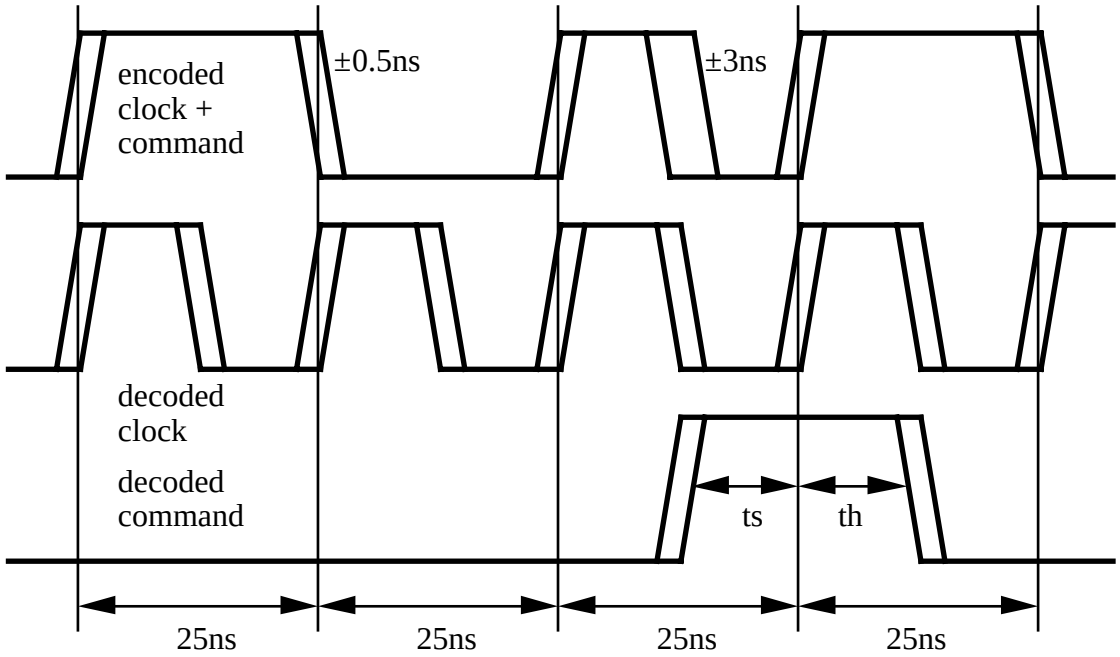


largest expected signal
high: 600μA
low: 0μA to 200μA
max step size: 600μA

smallest expected signal
high: 60μA
low: 0μA to 20μA
min step size: 40μA

- Propose to modify the specification to 20μA minimum high signal. Should check specification of worst case dim current (low signal). Claim is that the low signal should be completely negligible, and this specification is too conservative.
- Maximum input signal not well-analyzed, but could be closer to 800-1000μA.
- **Input noise requirements:** To achieve a BER of 10^{-12}, need signal/RMS noise ratio of 14:1. SCT specification is 25:1 to allow for additional noise sources (power supplies and coupling from other channels). The signal in this specification is the step size shown above, so the noise should be less than 1μA.

- **Output timing requirements:** Specified jitter on leading edge of extracted CK is +/-0.5ns, on high phase of CK is 12.5+/-1ns. Command decoding setup/hold timing relative to rising clock edge is specified as 8ns (ts/th below). Example below is from SCT specification:



- Note because of the BPM-encoded input stream for the DORIC, which is based on a 20MHz clock, it is critical to verify that the output CK from the DORIC has no significant odd/even variations in CK properties (every other CK edge is created by internal DLL) and no significant dependence on the data pattern modulated onto the input.
- **Power supply:** nominal supply voltage is 2.5V +/-0.2V, and consumption should be less then 20mA.

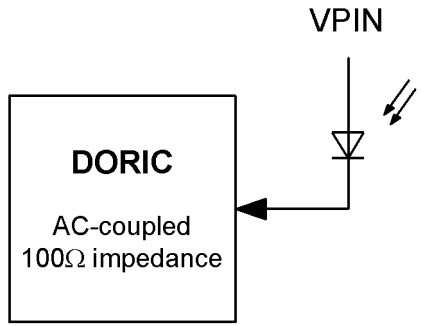
VDC:

- **Output Dim current:** (LVDS “0”) should be 1+/-0.5 mA
- **Output Bright current:** (LVDS “1”) should be 10mA nominal, and adjustable with VISET pin up to 20mA. Matching of Bright Current for a given VISET should be good (10-20% ?) since there is only one VISET line per opto-board.
- **Rise and Fall times:** output waveform rise and fall times should be roughly 1ns.
- **Current consumption:** should be independent of transmitted data value, and any transients at time of switching should be minimized. Real specification is that up to 14 VDCs must operate on the same substrate as 7 DORICs, without deteriorating the DORIC BER performance.
- **Power supply voltage:** nominal operating voltage should be 2.5V +/-0.2V, and total current consumption should not be more than 1.5 times the VCSEL current, or about 15mA nominal and 30mA worst case.
- **Output voltage:** must be capable of supplying 20mA output current to VCSEL with forward voltage of 2.3V, while still meeting rise/fall time specifications.

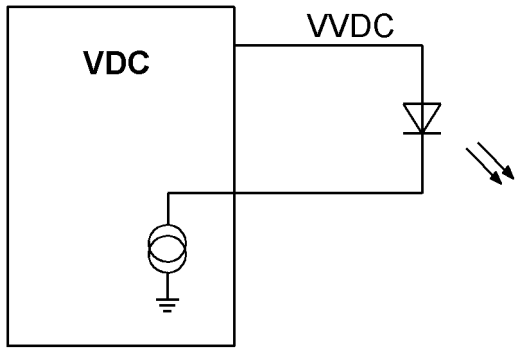
Open Issues in Opto-electronics

DORIC topology:

- Agreed to use a single-ended preamp (DORIC-I3). Since BPM-modulated input is DC-balanced, the preamp is AC-coupled. Presently, coupling caps are internal. Design is configured for common-anode operation. Use of this design in common-cathode mode would require either using a negative PIN bias supply, or moving the AC coupling outside the chip in order to withstand the full VPIN voltage of 10V.



Single-ended Common-Anode Design



Common-Anode Design

VDC topology:

- Electronics is configured for common-anode opto-elements. As long as the VCSEL forward voltage drop is less than the specified 2.3V, the design can be changed to a common-cathode design relatively easily by converting the NMOS current source to a PMOS current source.

Opto-electronics group wants to keep Common-Anode design.

Additional issue is VCSEL Forward Voltage:

- If the post-rad VCSEL forward voltage is too high for 0.25μ process (2.3V), then either the VDC can no longer supply enough current to provide the necessary light output, or a different topology needs to be considered.
- One proposal: a separate VVCSEL is defined in the services and brought in to the opto-boards in case it is needed. VDC would be tested in this configuration to make sure there were no problems. Note in this case, the I(VVCSEL) and I(VDC) would vary by large factors between “0” and “1” transmission...
- Based on the latest information from Taiwan, we do not expect to need this “fall-back” option, but it would be available in the system design in case it was needed.

Power Supply and Services Multiplicity:

- Propose small modification to opto-board 80-pin connector interface. The present two sense lines would be moved back to PP0 (little difference in quality of sensing), and replaced with VCSEL power supply lines VVCSEL and VVCSELRet.
- This gives a total of 10 power supply connections per opto-board (!!!). There is VPIN, VVCSEL, VISET, and 7 separate VVDC. Real issue is then how many of these supplies are routed separately out to PP2, and how many are routed all of the way to USA15.
- Opto-electronics group wants flexibility of running all 10 supplies from USA15. This implies minimizing voltage drops. VVDC will nominally be 2.5V on the opto-board, leaving very little margin for over-voltage. Not clear this works for 140m cable run.

- Alternate scheme connects all VVDC for one opto-board together at PP2, and supplies them from one regulator, using the sense lines for regulation. This would still give the flexibility to disconnect individual power lines at PP2 in a short access (would need detailed study). It would significantly reduce the complications for the power supplies (1 VVDC instead of 7 VVDC), and the Type 3 and 4 services.
- Finally, simplest scheme would connect everything together on PP0, and run a single VVDC cable from regulator at PP2. Personally remain unconvinced that the reliability of the opto-links is increased by having 7 VVDC (connectors more likely to fail than chips !)

Service Implications:

- Conductor sizing for going all the way to USA15 would require a total round-trip R budget of about 10Ω (700-1100mV voltage drop roundtrip).This would most likely mean AWG 28 for Type 1 and 2, for a total of about 5Ω roundtrip to PP2, and then AWG 20 for Type 3 and 4 for a total of about 7Ω for this part.
- Going to PP2 only could be done using AWG 30 (about 8Ω roundtrip from PP0 to PP2). Using a single VVDC would imply replacing 7 AWG 30 pairs with 1 AWG 22 pair (about 1Ω roundtrip resistance).
- Propose that we should agree on opto-board connector changes immediately, since this will affect next PP0 and opto-board prototypes. Would then suggest, if possible, to implement full AWG 28 services to PP2 for all VVDC, and assign a single regulator to each opto-board, with remote sensing from PP2 to PP0.